REMARKS

Applicant has reviewed the Office Action mailed on October 10, 2003, as well as the art cited. Claims 30 and 32 have been amended. Claims 1-32 are pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 form, listing all references that were submitted with the Information Disclosure Statement filed on April 8, 2003 and the Supplemental Information Disclosure Statement filed on April 8, 2003, marked as being considered and initialed by the Examiner, be returned with the next official communication.

Specification

The Specification was rejected to as failing to provide proper antecedent basis for the claimed subject matter. "Correction of ... in claim 32 is not supported either by the disclosure or the drawings."

Applicant has amended claim 32. As amended, Claim 32 is supported in the specification. In particular, please refer to Figure 1 and paragraph [0023] of the present application. Applicant respectfully requests the withdrawal of the rejection of claim 32

Rejections Under 35 U.S.C. § 112

Claim 32 was rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicant has amended Claim 32. As amended, Claim 32 is supported in the specification in such a way to enable one skilled in the art. Please refer to Figure 1 and paragraph [0023] of the present application. Applicant respectfully requests the withdrawal of the rejection of claim 32 under 35 USC § 112, first paragraph.

Rejections Under 35 U.S.C. § 102

Claims 1, 7, 12, 17, 30 and 31 were rejected under 35 USC § 102(b) as being anticipated by Nishimura, (U.S. Patent No. 5,990,715).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051, 10 (Fed. Cir. 1987). MPEP § 2131

Claim 1

In regards to independent Claim 1, Applicant respectfully traverses the Examiner's rejection of Claim 1 under 35 USC § 102(b). Claim 1 includes elements not taught by the Nishimura reference. For example, Claim 1 includes the element "a down converter channel coupled to receive each of the plurality of internal logic clock signals." The Nishimura reference does not teach "a down converter channel coupled to receive each of the plurality of internal logic clock signals." In particular, Nishimura reference relates to a semiconductor circuit having a voltage divider 30 that divides an input signal S1 into first and second output signals S2 and S3, wherein S3 is an inverted signal of S2. Please see Figures 2-4, and column 6 lines 10-43 of the Nishimura reference. Moreover, Nishimura (Figure-2 and column 5, lines 32-38) shows that only S2 is connected to a dummy delay circuit (34) while S3 is connected to a phase comparator (31). Hence, the Nishimura reference does not teach a down converter channel coupled to receive each of the plurality of internal logic clock signals. Accordingly, since not every element in Claim 1 is taught by the Nishimura reference, the Applicant respectfully requests the withdrawal of the rejection of Claim 1 under 35 USC § 102(b).

Moreover, since Claim 2-6 depends from and further define patentably distinct Claim 1 and for at least the reasons stated above, should also be allowed. In addition, since the Applicant believes the dependent claims are allowable for above reasons, not all rejections of said claims may have been addressed in this response. Hence, Applicant retains the right to address said rejections if a further response is required.

Claim 7

As noted above with regards to Claim-1, Nishimura does not teach "a down converter channel coupled to receive each of the plurality of internal logic clock signals." This element is also included in independent Claim 7. Accordingly, since not every element in Claim 7 is taught by the Nishimura reference, the Applicant respectfully requests the withdrawal of the rejection of Claim 7 under 35 USC § 102(b).

Moreover, since Claim 8-11 depends from and further define patentably distinct Claim 7 and for at least the reasons stated above, should also be allowed. In addition, since the Applicant believes the dependent claims are allowable for above reasons, not all rejections of said claims may have been addressed in this response. Hence, Applicant retains the right to address said rejections if a further response is required.

Claim 12

In regards to independent Claim 12, Applicant respectfully traverses the Examiner's rejection of Claim 12 under 35 USC § 102(b). Claim 12 includes elements not taught by the Nishimura reference. For example, Claim 12 includes the element "a down converter channel coupled to receive the plurality of internal logic clock signals." The Nishimura reference does not teach "a down converter channel coupled to receive **the plurality** of internal logic clock signals," as is disclosed and claimed in Claim 12 of the present application. The Nishimura reference relates to a semiconductor circuit having a voltage divider 30 that divides an input signal S1 into first and second output signals S2 and S3, wherein S3 is an inverted signal of S2. S2 is supplied to dummy delay circuit 34 and S3 is supplied to a phase comparator 31. Please see Figure 2 and column 5, lines 32-38 of the Nishimura reference. This is not what is claimed in Claim 12 of the present application as set out above. Since not every element in Claim 12 is taught by the Nishimura reference, Applicant respectfully requests the withdrawal of Claim 12 under 35 USC § 102(b).

Moreover, since Claim 13-16 depends from and further define patentably distinct Claim 12 and for at least the reasons stated above, should also be allowed. In addition, since the Applicant believes the dependent claims are allowable for above reasons, not all rejections of

said claims may have been addressed in this response. Hence, Applicant retains the right to address said rejections if a further response is required.

Claim 17

In regards to independent Claim 17, Applicant respectfully traverses the Examiner's rejection of Claim 17 under 35 USC § 102(b). Claim 17 includes elements not taught by the Nishimura reference. For example, Claim 17 includes the element "a down converter channel coupled to receive the plurality of internal logic clock signals." The Nishimura reference does not teach "a down converter channel coupled to receive **the plurality** of internal logic clock signals," as is disclosed and claimed in Claim 17 of the present application. The Nishimura reference relates to a semiconductor circuit having a voltage divider 30 that divides an input signal S1 into first and second output signals S2 and S3, wherein S3 is an inverted signal of S2. S2 is supplied to dummy delay circuit 34 and S3 is supplied to a phase comparator 31. Please see Figure 2 and column 5, lines 32-38 of the Nishimura reference. This is not what is claimed in Claim 17 of the present application as set out above. Since not every element in Claim 17 is taught by the Nishimura reference, Applicant respectfully requests the withdrawal of Claim 17 under 35 USC § 102(b).

Moreover, since Claim 18-20 depends from and further define patentably distinct Claim 17 and for at least the reasons stated above, should also be allowed. In addition, since the Applicant believes the dependent claims are allowable for above reasons, not all rejections of said claims may have been addressed in this response. Hence, Applicant retains the right to address said rejections if a further response is required.

Claim 30

Applicant has amended claim 30 to include the words "a plurality of internal logic clock signals of different frequencies." The Nishimura reference does not teach "a plurality of internal logic clock signals of different frequencies," as is claimed in claim 30 of the present application. As stated above, the Nishimura reference relates to internal logic clock signals S2 and S3 (as shown in Figure 2) having the same frequency but with a different phase (as shown in Figure 4,

5, 7 and 8; column 6, lines 42-44 of the Nishimura reference). Therefore, the Applicant respectfully requests the withdrawal of Claim 30 under 35 USC § 102(b).

Claim 31

Applicant respectfully traverses the Examiner's rejection of Claim 31 under 35 U.S.C. 102. Claim 31 includes the element "a phase comparator coupled to receive a first clock signal and ... a data channel coupled to receive the first clock signal ...." The Nishimura references does not teach ""a phase comparator coupled to receive **a first clock signal** and ... a data channel coupled to **receive the first clock signal** ...," as is disclosed and claimed in Claim 31 of the present application. Referring to Figure-2 of the Nishimura reference, the Nishimura reference relates to a divider circuit S3 outputting a signal S3 only to a phase comparator 31. Nishimura does not teach "a data channel coupled to **receive the first clock signal** ...." Since not every element in Claim 31 is taught by the Nishimura reference, Applicant respectfully requests the withdrawal of Claim 31 under 35 USC § 102(b).

Rejections Under 35 U.S.C. § 103

Claims 21, 24 and 27 were rejected under 35 USC § 103(a) as being unpatentable over Nishimura, (U.S. Patent No. 5,990,715).

Claims 2-4, 6, 8-10, 13-15, 18, 19, 22, 25, 26 and 29 were rejected under 35 USC § 103(a) as being unpatentable over Nishimura, (U.S. Patent No. 5,990,715) in view of Riordan et al. (U.S. Patent No. 5,317,601).

To establish a case of *prima facie* obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based in the applicant's

disclosure. *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir 1991). MPEP § 2143 - § 2143.03.

Claim 21

In regards to independent Claim 21, Applicant respectfully traverses the Examiner's rejection of Claim 21 under 35 USC § 103(a). Claim 21 includes elements not taught or suggested by the Nishimura reference. For example, Claim 21 includes the element "wherein each of the plurality of down converter channels is coupled to receive the plurality of internal logic clock signals." The Nishimura reference does not teach or suggest "wherein each of the plurality of down converter channels is coupled to receive the plurality of internal logic clock signals," as is disclosed and claimed in Claim 21 of the present application. The Nishimura reference relates to a semiconductor circuit having a voltage divider 30 that divides an input signal S1 into first and second output signals S2 and S3, wherein S3 is an inverted signal of S2. S2 is supplied to dummy delay circuit 34 and S3 is supplied to a phase comparator 31. Please see Figure 2 and column 5, lines 32-38 of the Nishimura reference. This is not what is claimed in Claim 21 of the present application as set out above. Since not every element in Claim 21 is taught or suggested by the Nishimura reference, Applicant respectfully requests the withdrawal of Claim 21 under 35 USC § 102(b).

Moreover, since Claims 22-24 depend from and further define patentably distinct Claim 21 and for at least the reasons stated above, should also be allowed. In addition, since the Applicant believes the dependent claims are allowable for above reasons, not all rejections of said claims may have been addressed in this response. Hence, Applicant retains the right to address said rejections if a further response is required.

Claim 27

Applicant traverses the Examiner's rejection of Claim 27 under 103(a). Claim 27 includes elements not taught or suggested by the Nishimura reference. For example, Claim 27 includes the element "...wherein each down converter channel is coupled to receive each of the plurality of internal logic clock signals and the control signal...." The Nishimura reference does

not teach or suggest "...wherein each down converter channel is coupled to receive each of the plurality of internal logic clock signals and the control signal...," as is disclosed and Claimed in Claim 27 of the present application. The Nishimura reference (at Figure-2 and column 5, lines 32-38) shows that S2 is connected to the dummy delay circuit (34) while S3 is connected to a phase comparator (31). Accordingly, the Applicant respectfully requests the withdrawal of the rejection of Claim 27 under 103(a).

Since Claim 28 and 29 depend from and further define patentably distinct Claim 27 and for at least the reasons stated above, should also be allowed. In addition, since the Applicant believes the dependent claims are allowable for above reasons, not all rejections of said claims may have been addressed in this response. Hence, Applicant retains the right to address said rejections if a further response is required.

Claims 25 and 26

In regards to independent Claims 25 and 26 Applicant respectfully traverses the Examiner's rejections of Claims 25 and 26 under 103(a). Not only has the Examiner failed to shown that the references teach every element of the respective claims, the Examiner has also failed to show a factual basis for modifying said references. Neither the Nishimura nor the Riordan et al. reference alone or in combination teach or suggest every element of respective claims 25 and 26. For example, claims 25 and 26 include the elements "when the one of the plurality of internal logic clock signals is in phase with the received sample clock, selecting a data signal that is clocked on the rising edge of the one of the plurality of internal logic clock signals" and "when the one of the plurality of internal logic clock signals is out of phase with the received sample clock, selecting the data that is clocked on the falling edge of the one of the plurality of internal logic clock signals" Neither the Nishimura nor the Riordan et al. reference teach or suggest these elements. Moreover, neither the Nishimura nor the Riordan et al. reference suggest to modify the reference to come up with what has been claimed in Claims 25 and 26 of the present application. Accordingly, the Applicant respectfully requests the withdrawal of the rejections of Claims 25 and 26 under 103(a).

Allowable Subject Matter

Claims 5, 11, 16, 20, 23 and 28 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant thanks the Examiner for the indication that claims 5, 11, 16, 20, 23 and 28 are allowable over the prior art if rewritten in independent form including all the limitations of the base claim and any intervening claims.

CONCLUSION

Applicant respectfully submits that claims **1-32** are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 332-4720.

Respectfully submitted,

Date: 1-12-4

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